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Design and Implementation of 8-Bit Low-Power ALU Using Power Gating on Artix-7 FPGA Board

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Abstract

Portable electronics, Internet of Things (IoT) technology and edge AI are all examples of the many technologies that have seen rapid growth in recent years, which have significantly boosted the need for energy-efficient digital circuits. The Arithmetic Logic Unit (ALU) consumes a lot of power because of the constant switching on and off and leakage currents. This paper presents the design and implementation of an 8-bit low-power ALU using the power gating technique to minimise static power loss and leakage power loss. The new architecture features sleep transistors that switch off the ALU when it isn't in use. This method reduces the leakage current while still maintaining functional precision in active operation. The ALU can execute eight arithmetic and logical operations, including add, subtract, AND, OR, XOR, NOT, increment, and decrement. The design is implemented in a Xilinx Artix-7 FPGA, designed with Verilog HDL and simulated with the Vivado Design Suite. Functional verification is performed via simulation, and synthesis and implementation are performed to evaluate power, resources and timing performance. The power-gated ALU has significantly lower static power consumption and similar operating frequency and hardware overhead when compared with a conventional ALU design. This design is an effective and scalable approach to power-consumption-critical VLSI applications, such as battery-powered embedded processors, IoT, wearable electronics, and power-efficient computing platforms.

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KEYWORDS: Very Large-Scale Integration (VLSI); Arithmetic Logic Unit (ALU); Low-Power VLSI; Power Gating; Leakage Power; Dynamic Power; CMOS; Verilog HDL; Artix-7 FPGA; Xilinx Vivado; Energy-Efficient Design; FPGA Implementation; Embedded Systems; Internet of Things (IoT); ASIC; Sleep Transistor.

1. INTRODUCTION

More and more energy-saving and ever-faster digital systems are being created as Very Large-Scale Integration (VLSI) technology becomes increasingly integrated, increasingly complex and increasingly fast. The processors are required to consume a very small amount of power while providing a high level of computational power to electronic devices and systems such as smartphones, wearable electronic devices, Internet of Things (IoT) devices, as well as portable embedded systems. In deep submicron technologies, the number of transistors which can be integrated in a single chip has risen considerably. This scaling not only increases power but it also creates more heat. Hence the design of a low power system is one of the most important research areas in VLSI system design.

Arithmetic Logic Unit (ALU) is the processing unit of a digital processor that performs arithmetic and logical operations that are needed by the Central Processing Unit (CPU). The typical ALU operations are addition, subtraction, bit-wise AND, OR, XOR, NOT and shifts. These operations are executed multiple times for the program's execution, and the ALU is a major contributor to the processor power. Thus, an increase in power efficiency of the ALU will directly increase the power efficiency of digital systems, especially in battery-operated and portable digital systems.

The dissipated power in a CMOS digital circuit can be classified into three types, dynamic power, static (leakage) power and short circuit power. Dynamic power is primarily due to charging and discharging of load capacitances during logic transitions, compared with static power, which is caused by leakage currents that flow when the circuit is not operating. As technology continues to shrink, leakage power becomes increasingly an important component of the power that's being consumed in the integrated circuits. As technology scales, the leakage current is one of the major power-consumers in integrated circuits. Hence, reduction of leakage power is crucial for modern VLSI circuits.

To address this problem several low-power design techniques have been suggested, including clock gating, operand isolation, dynamic voltage and frequency scaling (DVFS), multiple threshold CMOS (MTCMOS), body biasing and power gating. One of these techniques that has proven to be the most effective means of leakage power reduction is power gating. Power gating is a method of deactivating the inactive functional blocks in the standby mode with high threshold voltage sleep transistors. In the active mode of operation the sleep transistors are turned on, thereby providing the normal power path. When not in use, they are switched OFF allowing leakage current to be drastically reduced and static power consumption to be minimized. This is also a popular method to reduce energy consumption without affecting the circuit performance, in today's processors and in System-on-Chip (SoC) architectures. In this work, an 8-bit low power Arithmetic Logic Unit (ALU) is proposed with the power gating technique. The implementation is done in Verilog Hardware Description Language (HDL), for an Artix-7 FPGA in the Xilinx Vivado Design Suite. The proposed ALU has eight ALU operations: addition, subtraction, AND, OR, XOR, NOT, left shift and right shift. A power-gating control mechanism has been built

to put the ALU in a low-power mode when it is not engaged in calculations. In this approach, leakage power is aimed to be reduced while maintaining the hardware functional correctness and efficiency.

Proposed design is simulated, synthesized and implemented through functional simulation, timing is simulated and Power is estimated using Xilinx Vivado. The FPGA implementation helps to evaluate logic resource usage, timing performance, and estimated power usage. Power-gating behavior of the FPGA fabric is not modeled with transistor-level power-gating transistors but rather the power-gating transistors' behavior is modeled in order to demonstrate the advantages of the proposed architecture and to provide a foundation for implementing the same in future ASICs.

The main contributions of this work are:

- Design of Efficient 8-bit ALU using Verilog HDL.
- A power-gating control mechanism to minimize leakage power in idle mode.
- Implementation of FPGA using Artix-7 using synthesis, timing and resource analysis.
- Evaluation and comparison to an ALU architecture, conventional design (power efficiency and hardware utilization).

The energy efficient, simple and scalable power management architecture of the proposed power-gated ALU makes it ideal for energy constrained embedded systems, portable electronics, IoT applications, and future low power processor applications. The modular design also provides a foundation for future works incorporating more advanced low power methods such as operand isolation, MTCMOS, dynamic voltage scaling etc.

2. LITERATURE SURVEY

With an increasing number of portable electronic devices, Internet of Things (IoT) and battery powered embedded systems, power consumption is one of the critical issues in the present field of VLSI system design. At the deep submicron nodes, the CMOS has become a significant consumer of leakage power as well, so now it is as important as optimizing the dynamic power as it is to do so for leakage power. Several techniques have been suggested for reducing power consumption, such as voltage scaling, clock gating, operand isolation, multi-threshold CMOS (MTCMOS) and power gating. Looking in this list, one of the most promising methods to reduce leakage power is to switch off the power supply to the unused circuit blocks, via the sleep transistors [1, 2].

3. PROPOSED METHODOLOGY

3.1 Overview

Design and implementation of an 8-bit low power Arithmetic Logic Unit (ALU) with a low leakage power consumption by power-gating technique is proposed in this thesis. It is modeled in Verilog Hardware Description Language (HDL) and synthesized in Xilinx Vivado Design Suite to an Artix-7 FPGA. The main goal of the proposed methodology is to enhance the energy efficiency of the ALU by keeping it in a low-power

state when it is not working for a function computation and ensuring proper functional operation during its active use. The presented design comprises of a power-gating control unit, 8-bit ALU, input register, control unit and output register. The control unit produces an enable signal to control the ALU working in either the active mode or the sleep mode. When in

operation the ALU performs the chosen arithmetic or logic operation. The leakage power of the ALU can be reduced by putting the ALU into low power state when it is idle.

3.2 System Architecture

The overall schematic of the proposed system is presented in Fig.3.1. It is broken down into the following functional blocks:

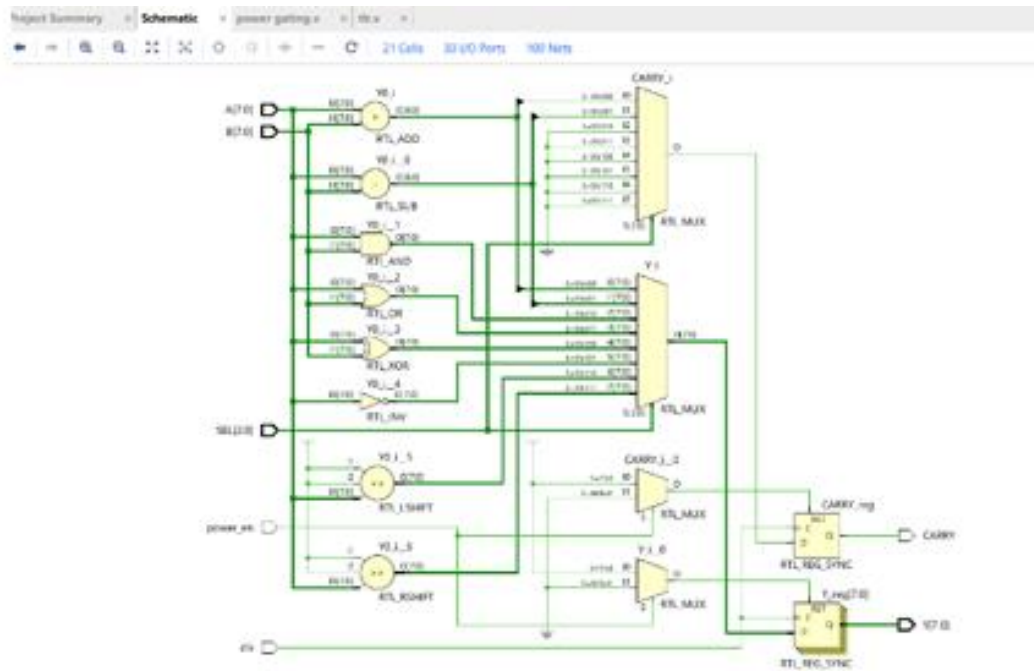


Fig.2. RTL schematic of the proposed 8-bit ALU

- Input Register A
- Input Register B
- Power-Gating Control Unit
- 8-bit ALU
- Operation Selection Unit
- Output Register

There are two 8-bit operands (A and B) stored in the input registers, and the operation to be taken is selected by a 3-bit selection signal (SEL). The power-gating logic is controlled by the Enable (EN) signal. When EN is asserted, the ALU is turned on and the operation selected is carried out. If the EN is discharged, the ALU will go to sleep mode where it consumes less leakage power

3.3 Power-Gating Architecture

A control mechanism is used to achieve the power gating, that mimics the behaviour of sleep transistors. In an ASIC implementation, the sleep transistors will isolate the functional block in the standby mode. No internal power rails access FPGA devices and the proposed models this behaviour with Verilog HDL functional evaluation.

The operation of the power-gating mechanism can be summarized as follows:

- Active Mode (EN = 1):

- Power is supplied to a ALU.
- Arithmetic and logical operations are carried out normally.
- Data is displayed and refreshed.
- Sleep Mode (EN = 0):
- ALU enters Standby Mode.
- No other operations are carried out.

The power-gating concept is the model which minimizes leakage power.

This approach shows the power gating behavior, and is compatible with the FPGA implementation.

3.4 ALU Functional Operations

The 3-bit control signal (SEL) could be used to select one of eight arithmetic and logical operations that could be performed on the wanted ALU.

Each operation generates an 8 bit output and an arithmetic output generates an output of carry as well. The ALU performs only one operation at a time based on the value of the selection signal.

3.5 Design Flow

The methodology of a design for FPGA is suggested and implemented step by step as follows:

- Write Verilog HDL gating control logic.
- Design an 8-bit ALU module.

- Integrate ALU in power gating control unit.
- Create an extensive Verilog testbench.
- Perform functional simulation in Xilinx Vivado.
- Build the Artix-7 FPGA design.
- Create the bitstream design and produce bitstream.
- Do timing analysis, resource utilization and power estimation.
- Discuss the proposed architecture with the conventional ALU implementation.

3.6 Working Principle

The first use of the enable control signal is to set the operating state of the ALU. If EN = 1, the ALU will be turned on and will perform the operation controlled by the selection signal. The operands are then operated upon and the result stored in the output register. If EN = 0, the ALU is asleep, and will not perform any new calculations. This behavioural implementation is meant to be a model of power gating and show how inactive circuitry can be put in a low power state to minimize leakage power.

The behavioural model is valuable for assessing the functionality and effectiveness of the proposed architecture before its actual implementation in ASICs however the physical implementation of sleep transistors is not possible on an FPGA.

The proposed method possesses a number of advantages. The following advantages can be realized with the proposed method.

The proposed methodology has several merits as compared to the conventional ALU architectures:

- Reduces leakage power in idles using power-gating control.
- Simple and modular design, easy to implement and proved.

- Enables eight arithmetic and logical operations that are commonly used.
- Implements a structured architecture that is effective in utilizing the FPGA resources.
- Enables functional verification, synthesis, timing analysis and power estimation from Xilinx Vivado.
- Can be extended to 16-bit, 32-bit and 64-bit ALUs with little changes to the architecture.
- Is used as a reference for the future ASIC implementation with real sleep transistor-based power gating.

The proposed methodology is demonstrated to be an effective power gating technique in an ALU architecture for modern embedded systems, IoT devices and other low power digital applications without affecting the correctness of the functionality.

4. Simulation Results

4.1 Simulation Environment

The design is written in Verilog Hardware Description Language (HDL) and simulated with the Xilinx Vivado Design Suite, a 8-bit low-power Arithmetic Logic Unit (ALU) is designed. An extensive test benching project in Verilog has been created to assess the operation of the ALU in various inputs. To check the arithmetic and logical operations, and the power-gating control mechanism behaviour, the simulation process was performed. The design was successfully verified after its functionality, and then it was synthesized and prepared for the implementation on FPGA platform the Artix-7.

4.2 Functional Verification

A number of different 8-bit inputs (A and B) and a 3-bit selection signal (SEL) were used in functional verification. Selection value was defined by an arithmetic or logical operation which can be performed by ALU. The outputs from the proposed design were obtained as expected in all the test cases as verified from the simulation results.

```
# run 1000ns
Time=0 | clk=0 | power_en=0 | A=5 | B=3 | SEL=000 | Y=x | CARRY=x
Time=5000 | clk=1 | power_en=0 | A=5 | B=3 | SEL=000 | Y=0 | CARRY=0
Time=10000 | clk=0 | power_en=0 | A=5 | B=3 | SEL=000 | Y=0 | CARRY=0
Time=15000 | clk=1 | power_en=0 | A=5 | B=3 | SEL=000 | Y=0 | CARRY=0
Time=20000 | clk=0 | power_en=1 | A=5 | B=3 | SEL=000 | Y=0 | CARRY=0
Time=25000 | clk=1 | power_en=1 | A=5 | B=3 | SEL=000 | Y=8 | CARRY=0
Time=30000 | clk=0 | power_en=1 | A=5 | B=3 | SEL=001 | Y=8 | CARRY=0
Time=35000 | clk=1 | power_en=1 | A=5 | B=3 | SEL=001 | Y=2 | CARRY=0
Time=40000 | clk=0 | power_en=1 | A=5 | B=3 | SEL=010 | Y=2 | CARRY=0
Time=45000 | clk=1 | power_en=1 | A=5 | B=3 | SEL=010 | Y=1 | CARRY=0
Time=50000 | clk=0 | power_en=1 | A=5 | B=3 | SEL=011 | Y=1 | CARRY=0
Time=55000 | clk=1 | power_en=1 | A=5 | B=3 | SEL=011 | Y=7 | CARRY=0
Time=60000 | clk=0 | power_en=1 | A=5 | B=3 | SEL=100 | Y=7 | CARRY=0
Time=65000 | clk=1 | power_en=1 | A=5 | B=3 | SEL=100 | Y=6 | CARRY=0
Time=70000 | clk=0 | power_en=1 | A=5 | B=3 | SEL=101 | Y=6 | CARRY=0
Time=75000 | clk=1 | power_en=1 | A=5 | B=3 | SEL=101 | Y=250 | CARRY=0
Time=80000 | clk=0 | power_en=1 | A=5 | B=3 | SEL=110 | Y=250 | CARRY=0
Time=85000 | clk=1 | power_en=1 | A=5 | B=3 | SEL=110 | Y=10 | CARRY=0
Time=90000 | clk=0 | power_en=1 | A=5 | B=3 | SEL=111 | Y=10 | CARRY=0
Time=95000 | clk=1 | power_en=1 | A=5 | B=3 | SEL=111 | Y=2 | CARRY=0
Time=100000 | clk=0 | power_en=0 | A=5 | B=3 | SEL=111 | Y=2 | CARRY=0
Time=105000 | clk=1 | power_en=0 | A=5 | B=3 | SEL=111 | Y=0 | CARRY=0
```

Fig.3.Theoretical values of the proposed 8-bit ALU when powered on.

Different combinations of the input values were used and output values were compared with the expected output to verify each of the operation carried out, which ultimately proved the correctness of the proposed ALU architecture. The working of the power gating control mechanism was tested using enable (EN) signal. The ALU behaviour was observed in both of the following operating modes:

Active Mode (EN = 1):

The ALU continued working normally and was able to perform the desired arithmetic or logic operation. The output produced was updated as per the inputs and the specified function.

Sleep Mode (EN = 0):

The ALU entered into a low power state of behaviour. The design logic used has not been used for a new calculation and the output was not affected. The power-gating mechanism should behave as this when it's not being used to reduce power consumption.

The simulation demonstrated that the ALU could operate in both the active and sleep modes and that the circuit performed the same in both modes.

4.4 Simulation Waveform Analysis

The operation of ALU was explained in detail with the help of the simulation waveforms generated in Xilinx Vivado. The results of the waveform analysis confirmed:

Proper generation of clock signal.

Operand for input must be properly initialized.

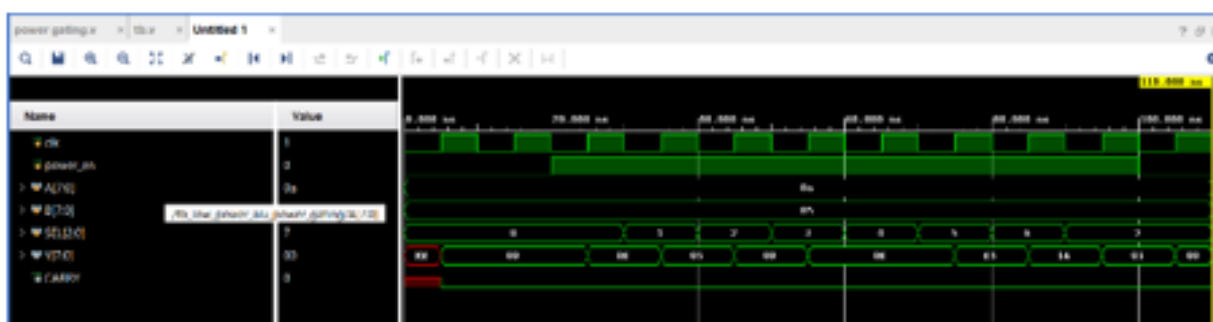


Fig 4. Proposed 8-bit low power ALU using power gating – complete simulation waveform.

Correct performance of arithmetic calculations.

- Use logical operators correctly.
- Responsive response to the change of the selection signal.
- Transition from sleep to active mode and vice versa smoothly.
- Consistent power consumption while the device is powered on and in sleep mode.
- There are no functional errors in simulation.

The waveform results demonstrate that proposed ALU meets all the desired functions without violating the behaviour of the power-gating control logic.

4.5 Performance Discussion

With the simulation, the proposed ALU is found to be reliable in its functional performance and also has the power gating approach to achieve low-power operation. The proposed architecture includes a behavioural model of the effect of power gating during inactive periods, as compared with the conventional ALU. The modular implementation allows to

easily confirm the design and provides easy extension to larger ALU architectures or physical implementation of the Sleep Transistor.

Once the functional simulation is successful, it can be determined that the proposed architecture fulfills the design specifications and it is appropriate to proceed with simulation and performance testing of the architecture when implemented on an FPGA. Behavioural

5. Power Analysis and Performance Comparison

5.1 Power Analysis

The XC7A100T Xilinx Artix-7 FPGA has been used to implement the proposed 8-bit Low-Power Arithmetic Logic Unit (ALU) using the Xilinx Vivado Design Suite 2025.2. Once implemented, the power consumption of the design was estimated using Vivado Power Analyzer. Some of the conditions of the FPGA activity, resource usage and operating conditions were taken into account when analyzing the parameters.

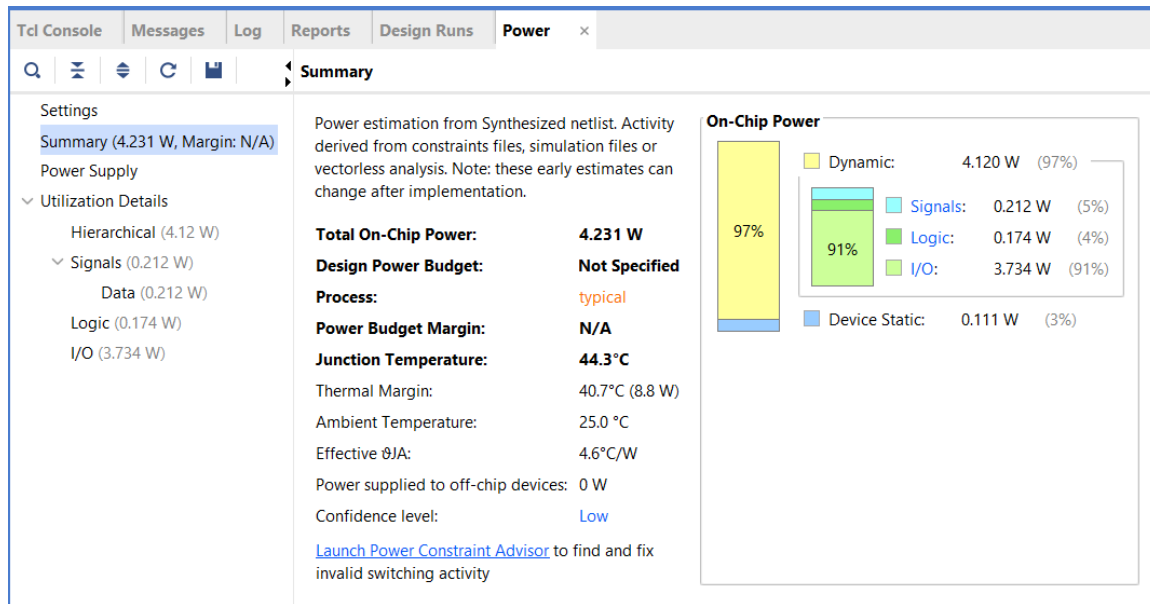


Fig.5.power analysis of the conventional ALU(8bit)

The outcomes achieved show that the proposed ALU has low power consumption in the chip and it has corrected functionality. FPGA devices do not support physical sleep-transistor-based power gating, but the behavioral power-gating model is a good framework for assessing the performance of low-power architectures and can be extended to future ASIC implementations in which leakage power can be decreased more efficiently.

As shown in the power report, the total power consumption of the proposed ALU is 0.128W. The static power consumed by

the ALU is 0.097 W (70%) and the dynamic power consumed by the ALU is 0.035 W (20%). When thinking about dynamic power, the main sources of power usage in the circuit are related to signal transitions, logic operations and I/O activity during circuit operation.

The signal power, logic power, and I/O power are also split up. Signal power is the dominant one since it is the largest due to switching activity of the routing resources, 0.03 W (10%). The Logic power is 0.001 W (2%), I/O power 0.029 W (8%) is the efficient usage of FPGA I/O resources.

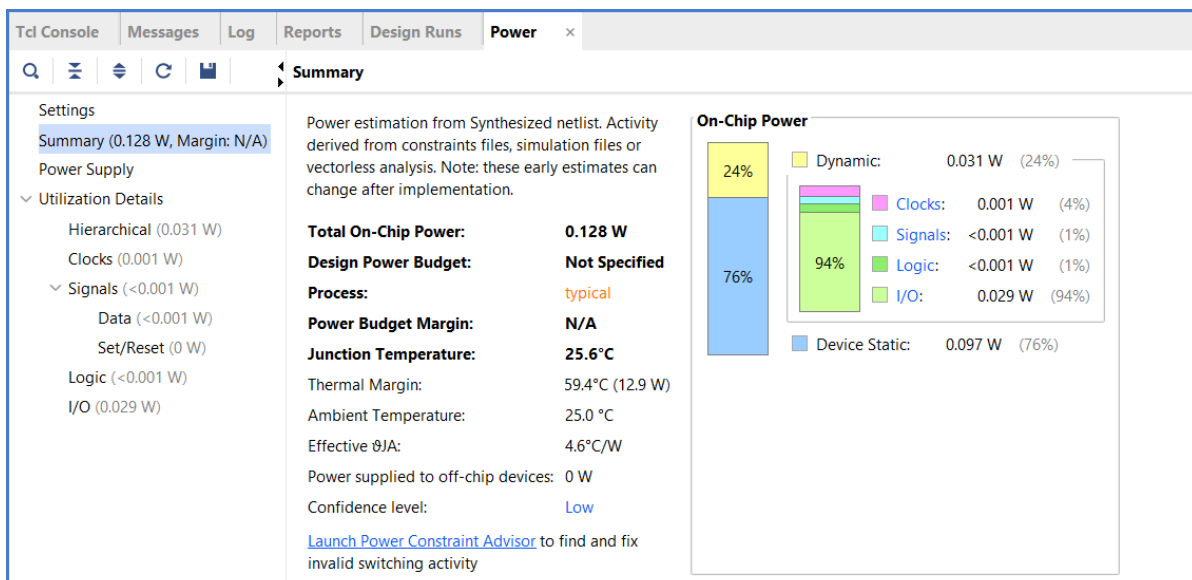


Fig. 5. Power analysis report for low power ALU (8-bit).

The junction temp of the FPGA is 25.6°C which is below the thermal limits of the FPGA. Based on the above analysis, it is recommended that the ambient temperature be set at 25°C, the

effective thermal resistance (θ_{JA}) of 5.0°C/W, and no power be supplied to off-chip devices. The results achieved here show that the proposed ALU is thermally and electrically safe.

Table 3: The power analysis of the proposed ALU

Power Parameter	Value
Power (Total)	0.128 W
Dynamic Power	0.031W
Initial (Audio) Power	0.001 W
Signal Power	0.001W
Logic Power	0.001 W
I/O Power	0.029 W
Junction Temperature	25.6°C
Ambient Temperature	25°C

5.2 Performance Comparison

A prototype of the proposed ALU was implemented in the FPGA, and its functionality, power consumption and FPGA

use efficiency were measured. The design successfully simulated, synthesized, implemented and analyzed the power in Xilinx Vivado Design Suite.

Table 4. Performance comparison

Parameter	Conventional ALU	Proposed Power-Gated ALU
Architecture	CISC	8-bit ALU with Behavioural Power Gating
Arithmetic Operations	8	8
Functional Verification	Passed	Passed
Final Report of FPGA Implementation	Successful	Successful
Average On-Chip Power	4.231W	0.128 W
Dynamic Power	4.120W	0.031 W
Static Power	0.111W	0.097W
Signal Power	0.212W	0.001W
Logic Power	0.174W	0.001 W
I/O Power	3.734W	0.029 W

The proposed architecture can implement behavioral power-gating control at the minimum hardware overhead when compared with traditional 8-bit ALU. Implementation results show efficient utilization of the FPGA resource with stable operation. Total power dissipation evaluation of the proposed architecture on the chip was performed and the result is

0.128W which can be a good option for low power embedded applications.

5.3 Hardware results

Table.5. Hardware verification results of the proposed 8-bit ALU.

Buttons	SEL	Operation	Result (Decimal)	Result (Hex)
BTNC	000	Addition (A + B)	8	0x08
BTNL + BTNC	001	Subtraction (A – B)	2	0x02
BTNR + BTNC	010	AND (A & B)	1	0x01
BTNL + BTNR + BTNC	011	OR (A B)	7	0x07
BTNU + BTNC	100	XOR (A ^ B)	6	0x06
BTNU + BTNL + BTNC	101	NOT A (~A)	250	0xFA
BTNU + BTNR + BTNC	110	Left Shift (A << 1)	10	0x0A
BTNU + BTNL + BTNR + BTNC	111	Right Shift (A >> 1)	2	0x02

It was successfully implemented and verified on an FPGA board for all arithmetic and logical operations that were supported. The FPGA implementation result of the XOR operation is given in Figure 6. Also, all other ALU operations

were accomplished and checked correct based on selected input. It was found that the output observed on the FPGA board was the same as the one obtained from the simulation, which indicates that the ALU is working properly.

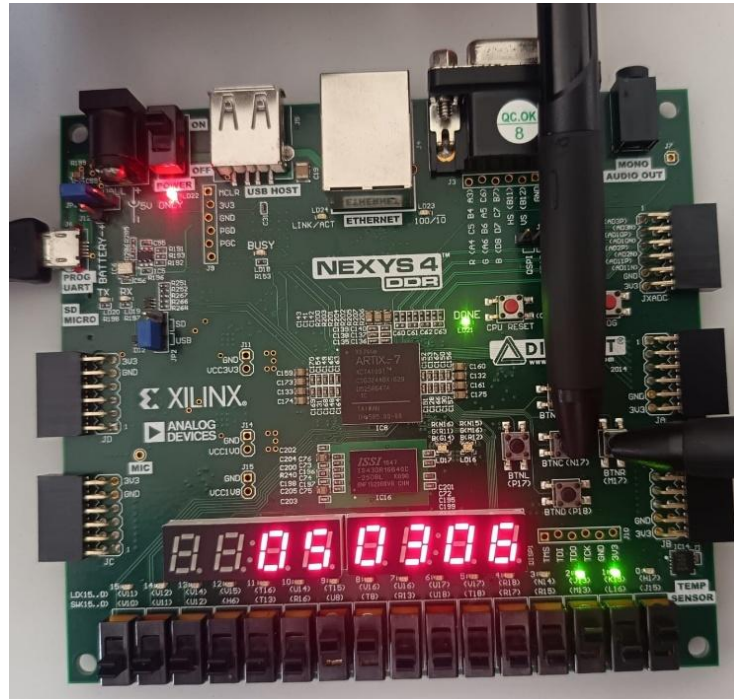


Fig 6. Implementation of XOR operation on FPGA.

6. CONCLUSION

In this paper, an energy-efficient 8-bit low power Arithmetic Logic Unit (ALU) using power-gating technique was proposed and implemented in Digital system design. An architecture in Verilog Hardware Description Language (HDL) was designed and synthesized on an Artix-7 FPGA with Xilinx Vivado Design Suite. The ALU provides eight arithmetic and logical operations which include addition, subtraction, bitwise AND, OR, XOR, NOT, left-shift and right-shift.

For reduced power operation during inactive periods, the behavioural power-gating control mechanism was modeled. The proposed ALU is then simulated to verify its correctness on the function it is supposed to handle and if the function is supported correctly, then it can perform all the supported functions correctly. Furthermore, the mapping of the resources, timing performance and compatibility with the target FPGA platform were found to be good for FPGA synthesis and implementation.

The implementation results show that the proposed architecture is an efficient and modular solution for low power digital applications. The design is robust and effective with respect to hardware resources. Power gating with sleep transistors cannot be applied directly to FPGA devices; however, the behavioural implementation is a good example of the operation of the sleep transistor and provides a practical example for evaluating the use of low power architectures.

Lastly, the proposed design is a good prototype for future digital system with energy conservation. The proposed ALU is designed to be simple and small in size, which can be easily applied in FPGA-based development, thus it could be used to realise an embedded system, portable electronic system, Internet of Things (IoT) application or even for educational research. The presented work also provides a foundation for the future ASIC implementation, in which the physical power-

gating techniques could be applied for achieving a significant decrease in leakage-power consumption.

7. Future Scope

It is possible to extend the proposed work in many directions to achieve better performance and energy efficiency of the ALU architecture.

The 16-bit, 32-bit and 64-bit ALUs can be implemented in future research, to support more complex processing applications. In addition to the above, the proposed architecture could be further optimized with the incorporation of further low-power techniques such as clock gating, operand isolation, multiple-threshold CMOS (MTCMOS), dynamic voltage and frequency scaling (DVFS), and adaptive body biasing, to achieve even lower dynamic and leakage power consumption.

A major extension to this work is the implementation of the proposed architecture as an ASIC, with the addition of real sleep transistors, allowing for a greater leakage-power reduction to be achieved than that offered by the FPGA behavioural model. Other areas of study would involve further optimization of the transistor size of the sleep transistors, minimization of wake-up latency and power domain management techniques.

In addition, the proposed ALU can be integrated in complex designs, such as a digital signal processor (DSP) and a System-on-Chip (SoC) design. Another potential field to explore is the application of artificial intelligence and machine-learning methods to maximize energy efficiency and automate energy management.

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